

A

B

C

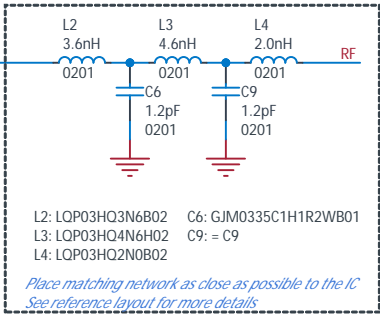
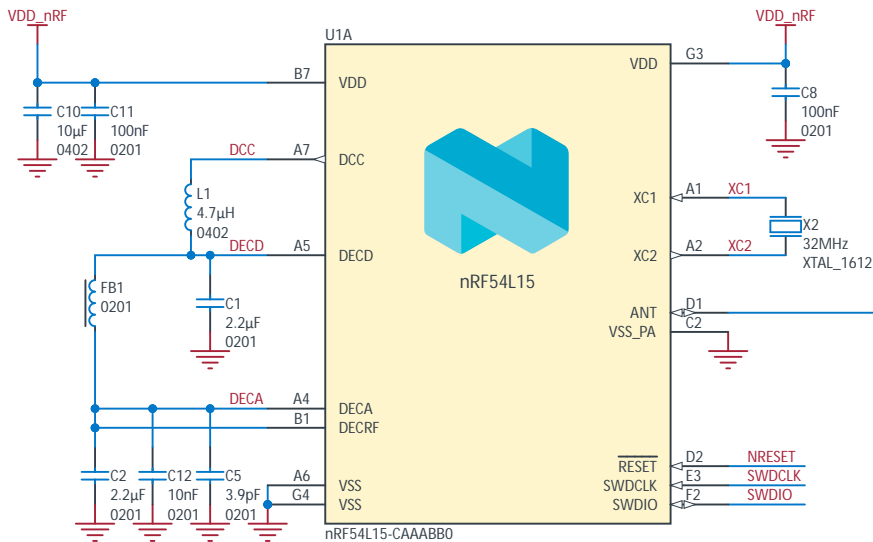
D

A

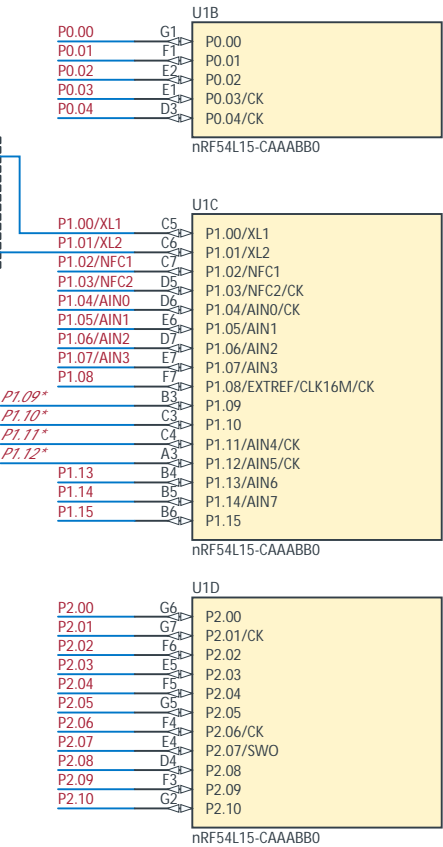
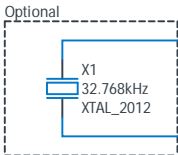
B

C


D



Preliminary matching network for nRF54L15  
Engineering B. Updates should be expected to recommended component values prior to SoC entering mass production. Contact your Nordic Sales Representative for the latest information.



\* Please refer to chip-level errata before using GPIO pins P1.09, P1.10, P1.11 and P1.12

|   |  |                  |   |
|---|--|------------------|---|
| Title<br>nRF54L15-caaa Reference Layout |  |                  |  |
| Size<br>A4                              | PCB Assembly Number<br>nRF54L15 Reference Layout | Revision<br>v0.4 |   |
| Date: 01.11.2024                        |  | Sheet 1 of 1     |   |
| File: nRF54L15-caaa_config1.SchDoc      |  | Drawn By: STL1   |   |
| Classification: PUBLIC                  |  |                  |   |